

Comparison of 60GHz CSRRs Ground Shield and Patterned Ground Shield On-chip Bandpass Filters Designed for 0.18 μ m CMOS Technology

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Abstract: This paper present on-chip open loop resonators 60GHz bandpass filters fabricated with the complementary metal-oxide semiconductor (CMOS) 0.18 μ m technology. Both filters have different ground shield placed at the lowest metal, M1. The first filter is designed with patterned ground shield below while the other filter with complementary split ring resonators (CSRR) as ground shield. The purpose of this research is to examine the best ground shield that can be used and employed to enhance the performance of the filter. Design simulation is conducted with electromagnetic simulator tools. It shows that, filter with CSRR as ground shield produce better results with $S_{21} = -2.682\text{dB}$, 3-dB bandwidth = 10.8GHz compare to patterned ground shield with $S_{21} = -2.77\text{dB}$, 3-dB bandwidth = 14GHz with both have good return loss.

Keywords: bandpass filter, CMOS, CSRRs, open loop resonators

I. Introduction

In modern RF wireless communication systems, filters constructed with CMOS technology process become great importance for enabling the integration of the millimeter-wave system on a single chip (SoC). Compactness and lightweight are required in the realization of the BPF. Besides that, maximal loss inside the pass region, minimal attenuation in the reject/stop regions and the transition region are also necessary to be considered in design of respective filters. Although many researches have been conducted for the development of on-chip passive filters in the unlicensed frequency band, these filters suffered from high insertion loss, occupy larger chip area and more bandwidth [1-3] makes it difficult to be used in real implementation. BPF is an indispensable cascade component in the transmission system, thus decreasing the insertion loss and bandwidth allocated are of great importance.

II. CSRRs and Patterned Ground shield

Both filters designed employed the open loop resonators structure placed at the top metallization layer, M6 of the CMOS 0.18 μ m technology. To achieve high selectivity and low insertion loss in this filter design, cross coupling topology with quasi-elliptic response indicated by 4th order cross-coupled filter with a pair of transmission zeros at finite frequencies is applied. The length of the resonator was estimated to be 1250 μ m with line width of 10 μ m which gives 50 Ω impedance on the substrate. Fig. 1 shows the filter design with employed folded structure.

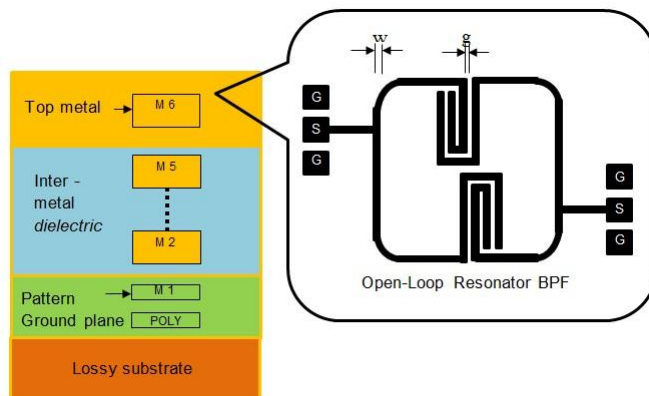


Fig. 1 0.18 μ m CMOS metal layers and filter structure with folded structure

Complimentary Split Ring Resonator (CSRR) is the contrast structure of split ring resonator (SRR) which has a connected metallic ground plane extends all over the structure as shown in Fig. 2(a), the width of the rings are $5\mu\text{m}$ and space of $5\mu\text{m}$ respectively. Two gaps are designed opposite each other in one side of the ring. This gap would make the electric field concentrated within the split gap and smaller value of distributed capacitance resulted. Thus more power is radiated inside the ring [4].

This structure is suitable as the ground structure because dielectric substrate with a significant dependence of its permittivity on an external electrostatic field can be easily tuned. The complementary of a planar metallic structure is obtained if the metal parts of the original structure are replaced with apertures, and the apertures with metal plate. The thickness of the metal plate is zero and its conductivity is infinite due to symmetrical configuration, thus the apertures behave as perfect magnetic conductors [5]-[6]. Therefore the original structure and its complementary are effectively dual.

Other than CSRR as ground, patterned ground shield (PGS) has recently been designed to improve the insertion loss and increase the performance of the filter. PGS could increase the Q-factor to almost 50% of the inductor. Fig. 2(b) shows the proposed PGS with slots orthogonal to the spiral designed to increase the resistance of the image current. The slots act as open circuit to cut off the path of the induced loop current. It should be narrow as possible so that the vertical electric field cannot leak through the PGS into the substrate below it. The ground strips act as the termination for the electric field. The shield should be strapped with the top layer metal to provide a low impedance path to ground. The main reason is to prevent negative mutual coupling and minimizing the impedance to ground. As the magnetic field passes through the PGS, its intensity is weakened due to the skin effect. This directly causes a decrease in the inductance since the magnetic flux is lessened in the space occupied by the ground shield layer [7-8]. The size of the strips and slot are $4\mu\text{m}$ and $5\mu\text{m}$ respectively.

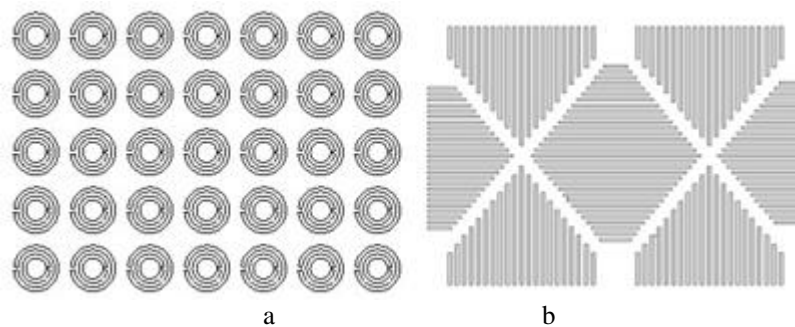


Fig . 2 CSRRs as ground shield and patterned ground shield

Simulation had been carried out to examine the effect of placing of SRRs on either metal 5 (M5) or metal 2 (M2), and the result is shown in Fig. 3. It is shown that, at M5, BPF shows over-coupled condition. It occurs because the spacing between the SRRs and the folded structure has to be adjusted critically. Over coupled condition or so-called double humping exists when M5 and M6 are too close together resulted very wide response. Thus, by placing SRRs on M2, (placing further apart from M6), wider coupling occurred and this results much sharper response. There is a limit distance between SRRs and folded filter structure to produce critical coupling. Proper optimization could produce better results and coupling coefficient.

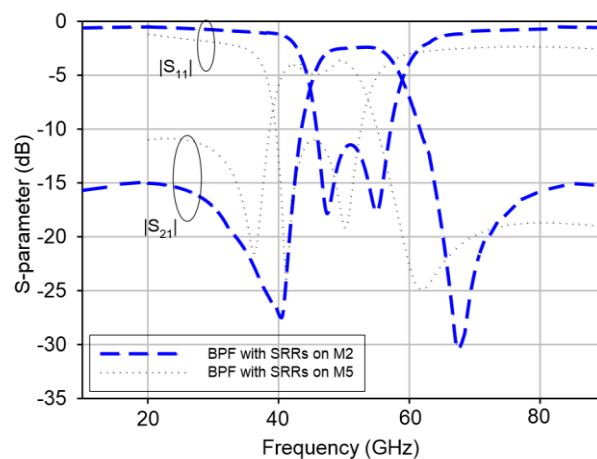


Fig. 3 Simulation results on the effect of placing SRRs either on M5 or M2 of CMOS layer

III. BPF Structure

The structures of both filters are illustrated in Fig. 4 using 3D EM preview of Agilent ADS Momentum 2009. The chip are for both filters are 0.651mm^2 and 0.527mm^2 respectively as shown in Fig. 5 and Fig. 6.

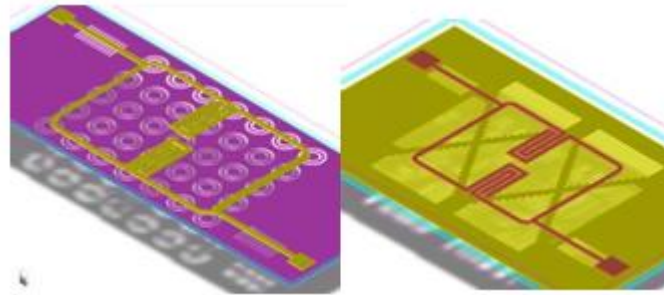


Fig. 4 3D view of BPF with CSRR and PGS as ground

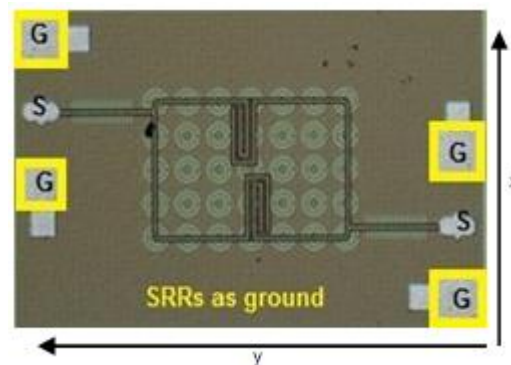


Fig. 5 CSRR as ground shield (Chip size, $xy=0.527\text{mm}^2$)

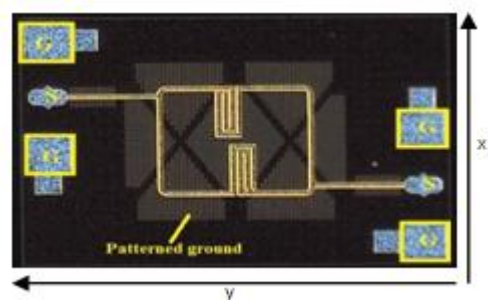


Fig. 6 Patterned ground shield (Chip size, $xy = 0.527\text{mm}^2$)

IV. Results And Tables

The measurement for chips design was then conducted using Agilent Vector Network Analyzer (PNA-E8361C) which gives measurement up to 70GHz only. Whilst, the simulation results is calculated using Agilent ADS 2009. The results are shown in Fig. 7 and Fig. 8 respectively. It shows that BPF with CSRR produce results of insertion loss of 2.682dB compare to simulation result of 3.0dB, better return loss, and 3-dB bandwidth of 10.8GHz with center frequency of 56.0GHz. Meanwhile, for the BPF with PGS as ground, insertion loss is 2.77dB, better return loss but 3-dB bandwidth of 14GHz with simulation results produce good agreements results compare to the measurement result. The results are summarized in Table 1 shows the summary of the designed filters.

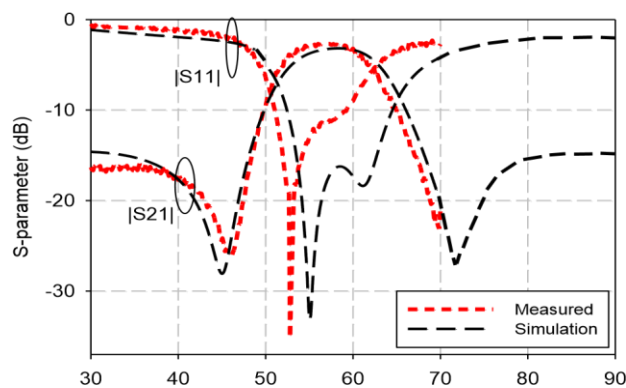


Fig. 7 Measurement and simulation results for BPF with CSRR as ground

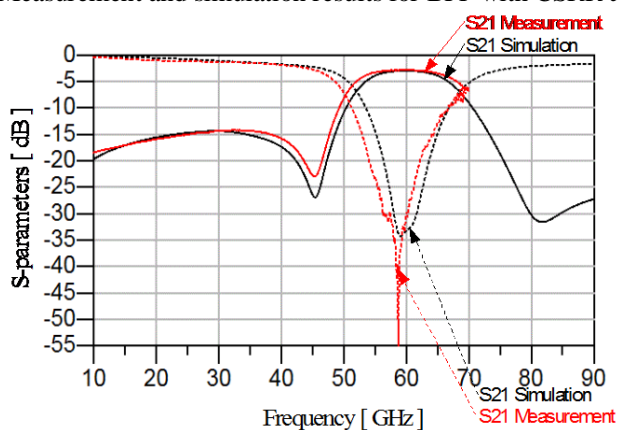


Fig. 8 Measurement and simulation results for BPF with PGS as ground

Table 1 Summary of results for both designed filters

Design	S21 [dB]	S11 [dB]	Center frequency [GHz]	Bandwidth [GHz]	Chip size [mm]
BPF with CSRRs as ground	-2.682	<-35	56.0	10.8	0.651
BPF with patterned ground	-2.77	<-20	57.5	14	0.527

V. Conclusion

This paper presents BPFs with patterned ground shield and CSRR as the ground metal. Both experimental and measurement results show good approximation to each other.

Although the patterned ground shield produce 2.77dB insertion loss, compare to CSRR which is 2.682dB but it produce bigger bandwidth for the 60GHz applications. It shows that CSRR is well optimized as the ground metal for the filter design. Besides, CSRRs produce much narrower bandwidth, 10.8GHz compare to patterned ground with only 14GHz. Thus, it is the best design to be applied for SoC technology.

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